REMARKS

The Office Action mailed March 28, 2002, has been received, and reviewed. Claims 1 through 10 are currently pending in the application. Claims 3-6 and 8-10 are allowed. Claims 1, 2, and 7 stand rejected. Applicants have amended claim 2 to improve antecedent basis in the body of the claim and respectfully request reconsideration of the application as amended herein.

Possible Omission or Miscitation of Reference by theOffice

Applicants respectfully note that a Form PTO-892 listing certain U.S. and foreign patent documents was enclosed with the outstanding Office Action. However, the Office Action, page 6, paragraph 12, referenced an "IBM technical bulletin Vol. 30 No. 3 discloses an On-chip decoupling capacitor for VLSI chips," yet no copy of the document was provided nor was the document listed on the form PTO-892. Unfortunately, since no page numbers were given, and the referenced technical disclosure bulletin contains numerous documents, Applicants are uncertain as to what document the Office is referencing in the Office Action. The confusion is compounded by the fact that Applicants cited two IBM Technical Disclosure Bulletins from Vol. 30 in their Supplemental Information Disclosure Statement filed January 9, 2002 and, as noted below, the Office has not made this Supplemental Information Disclosure Statement of Record (see below). Thus, Applicants surmise that the missing reference noted in the Office Action may have been cited from their PTO-1449, and thus may be not a separate document discovered by the Examiner, but a document cited by Applicants and inadvertently misidentified by the Examiner in the Office Action. Clarification is respectfully requested and, if there is indeed a new reference discovered by the Examiner, that such be identified on a Form PTO-892 and a copy thereof supplied to Applicants' undersigned attorney.

Information Disclosure Statement

Applicants note the filing of a Supplemental Information Disclosure Statement herein on January 9, 2002 and note that no copy of the PTO-1449 was returned with the outstanding Office

Action. Applicants respectfully request that the information cited on the PTO-1449 be made of record herein and would appreciate receiving a copy of the PTO-1449 as initialed by Examiner with the next office action. Should the Information Disclosure Statement, PTO-1449 and copies of the cited references have failed to reach the Examiner, Applicants' undersigned attorney would be happy to have a duplicate set hand-delivered to the Examiner.

1. Terminal Disclaimer

Applicants acknowledge and thank the Examiner for review and entry of the terminal disclaimer filed on January 9, 2002.

2. 35 U.S.C. § 102 Anticipation Rejections

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

3. Claim 1 Anticipation Rejection Based on Japanese Patent No. JP 61-73367 to Matsumoto

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Matsumoto (Japanese Patent No. JP 61-73367). Applicants respectfully traverse this rejection, as hereinafter set forth. It appears that examiner may have misunderstood the element of "a carrier substrate" in the present application. The carrier substrate element clearly refers to a separate substrate, such as a SIMM or SIP module, to which the semiconductor device is secured and operably coupled. The carrier substrate is a different element than the semiconductor device, as is clear from the separate recitation thereof in the claim as well as the recitation of "a semiconductor device secured and operably coupled to the carrier substrate . . . ." (emphasis added). In other words, while the Examiner may have misapprehended that Applicants are claiming the forming

of integrated circuitry or "semiconductor device" on an active surface of a semiconductor substrate, such as a semiconductor die, and that the recited "carrier substrate" is a semiconductor substrate, this is clearly not the case. Element 1 of the Matsumoto reference refers to the substrate of the semiconductor device and applicants can find no reference in Matsumoto to a carrier substrate as recited in claim 1 of the present application. As such, Matsumoto does not set forth each and every element in claim 1 and therefore does not anticipate claim 1.

4. Claim 1 Anticipation Rejection Based on U.S. Patent No. 4,477,736 to Onishi

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onishi (U.S. Patent No. 4,477,736). Applicants respectfully traverse this rejection, as hereinafter set forth. Again as stated previously, the recited carrier substrate element refers to a separate substrate, such as a SIMM or SIP module, to which the semiconductor device is secured and operably coupled. The carrier substrate is a different element than the semiconductor substrate of the semiconductor device. Element 11 of the Onishi reference refers to the substrate of the semiconductor device and applicants can find no reference in Onishi to a carrier substrate as recited in claim 1 of the present application.

Additionally, the capacitors in the Onishi reference have one terminal connected between an internal signal of the semiconductor device with the second terminal connected to VDD of the semiconductor device for the first capacitor and VSS of the semiconductor device for the second capacitor. This is clearly a different configuration than what is recited in claim 1 of the present application with the clause, "on-chip capacitor being operably coupled between the active circuit devices and the **carrier substrate**" (emphasis added).

For these reasons, the Onishi reference does not set forth each and every element in claim 1 and therefore does not anticipate claim 1.

5. Claim 1 Anticipation Rejection Based on U.S. Patent No. 4,720,467 to Muggli et al.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Muggli et al. (U.S. Patent No. 4,720,467). Applicants respectfully traverse this rejection, as hereinafter set forth. As stated previously, the carrier substrate element refers to a separate substrate, such as a SIMM or SIP module, to which the semiconductor device is secured and operably coupled. The carrier substrate is a different element than the semiconductor substrate of the semiconductor device. Element 21 of the Muggli reference refers to the substrate of the semiconductor device and applicants can find no reference in Muggli to a carrier substrate as recited in claim 1 of the present application.

Additionally, the Muggli reference does not define any connections for the capacitors 20. Whereas, in the present application a connection is recited in claim 1 with the clause, "on-chip capacitor being **operably coupled between the active circuit devices and the carrier substrate**" (emphasis added).

For these reasons, the Muggli reference does not set forth each and every element in claim 1 and therefore does not anticipate claim 1.

6. Claim 2 Anticipation Rejection Based on Japanese Patent No. JP 61-73367 to Matsumoto

Claim 2 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Matsumoto (Japanese Patent No. JP 61-73367). Applicants respectfully traverse this rejection, as hereinafter set forth. As stated previously, the carrier substrate element refers to a separate substrate, such as a SIMM or SIP module, to which the semiconductor device is secured and operably coupled. The carrier substrate is a different element than the semiconductor substrate of the semiconductor device. Element 1 of the Matsumoto reference refers to the substrate of the semiconductor device and applicants can find no reference in Matsumoto to a carrier substrate as defined in the present application. Claim 2 of the present application, on the other hand, contains the clause, "when the semiconductor device is **operably coupled to the carrier substrate**" (emphasis

added). As such, Matsumoto does not set forth each and every element in claim 2 and therefore does not anticipate claim 2.

7. Claim 2 Anticipation Rejection Based on U.S. Patent No. 4,477,736 to Onishi

Claim 2 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onishi (U.S. Patent No. 4,477,736). Applicants respectfully traverse this rejection, as hereinafter set forth. As stated previously, the carrier substrate element refers to a separate substrate, such as a SIMM or SIP module, to which the semiconductor device is secured and operably coupled. The carrier substrate is a different element than the semiconductor substrate of the semiconductor device. Element 11 of the Onishi reference refers to the substrate of the semiconductor device and applicants can find no reference in Onishi to a carrier substrate as defined in the present application. Claim 2 of the present application, on the other hand, contains the clause, "when the semiconductor device is **operably connected to the carrier substrate**" (emphasis added).

Additionally, the capacitors in the Onishi reference have one terminal connected between an internal signal of the semiconductor device with the second terminal connected to VDD of the semiconductor device for the first capacitor and VSS of the semiconductor device for the second capacitor. This is clearly a different configuration than what is recited in claim 2 of the present application with the clause, "the capacitor being operably coupled to the active circuit devices to provide filtering capacitance for the semiconductor device **when the semiconductor device is operably connected to the carrier substrate**" (emphasis added).

For these reasons, the Onishi reference does not set forth each and every element in claim 2 and therefore does not anticipate claim 2.

8. Claim 2 Anticipation Rejection Based on U.S. Patent No. 4,720,467 to Muggli et al.

Claim 2 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Muggli et al. (U.S. Patent No. 4,720,467). Applicants respectfully traverse this rejection, as hereinafter set forth. As stated previously, the carrier substrate element refers to a separate substrate, such as a

SIMM or SIP module, to which the semiconductor device is secured and operably coupled. The carrier substrate is a different element than the semiconductor substrate of the semiconductor device. Element 21 of the Muggli reference refers to the substrate of the semiconductor device and applicants can find no reference in Muggli to a carrier substrate as defined in the present application. Claim 2 of the present application, on the other hand, contains the clause, "when the semiconductor device is **operably coupled to the carrier substrate**" (emphasis added).

Additionally, the Muggli reference does not define any connections for the capacitors 20. However, in the present application a connection is recited in claim 2 with the clause, "the **capacitor being operably coupled to the active circuit devices** to provide filtering capacitance for the semiconductor device **when the semiconductor device is operably connected to the carrier substrate**" (emphasis added).

For these reasons, the Muggli reference does not set forth each and every element in claim 2 and therefore does not anticipate claim 2.

9. Claim 7 Anticipation Rejection Based on Japanese Patent No. JP 58-77251 to Kachi

Claim 7 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Kachi (Japanese Patent No. JP 58-77251). Applicants respectfully traverse this rejection, as hereinafter set forth. The capacitor 4 referred to in Fig. 2 of the Kachi reference is a chip capacitor, which is a separate device, affixed to the lead frame of the package. The capacitor in the present invention, on the other hand, is an integral part of the semiconductor substrate as evidenced by the clause in claim 7 of the present application, "at least one capacitor on the semiconductor substrate, at least a portion of the **at least one capacitor being formed on the active area**" (emphasis added).

Additionally, as stated previously, the carrier substrate element refers to a separate substrate, such as a SIMM or SIP module, to which the semiconductor device is secured and operably coupled. Applicants can find no reference in Kachi to a carrier substrate. Claim 7 of the present application, on the other hand, contains the clause, "when the semiconductor device is operably connected to power and ground of the **carrier substrate**" (emphasis added).

For these reasons, the Kachi reference does not set forth each and every element in claim 7 and therefore does not anticipate claim 7.

10. Claim 7 Anticipation Rejection Based on U.S. Patent No. 4,477,736 to Onishi

Claim 7 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Onishi (U.S. Patent No. 4,477,736). Applicants respectfully traverse this rejection, as hereinafter set forth. As stated previously, the carrier substrate element refers to a separate substrate, such as a SIMM or SIP module, to which the semiconductor device is secured and operably coupled. The carrier substrate is a different element than the semiconductor substrate of the semiconductor device. Element 11 of the Onishi reference refers to the substrate of the semiconductor device and applicants can find no reference in Onishi to a carrier substrate as defined in the present application. Claim 7 of the present application, on the other hand, contains the clause, "when the semiconductor device is **operably connected to power and ground of the carrier substrate**" (emphasis added).

Additionally, the capacitors in the Onishi reference have one terminal connected between an internal signal of the semiconductor device with the second terminal connected to VDD of the semiconductor device for the first capacitor and VSS of the semiconductor device for the second capacitor. This is clearly a different configuration, and solves a different problem than the structure recited in claim 7 of the present application, including "**at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefor** when the semiconductor device is **operably connected to power and ground of the carrier substrate**" (emphasis added).

For these reasons, the Onishi reference does not set forth each and every element in claim 7 and therefore does not anticipate claim 7.

11. Applicants acknowledge and thank the examiner for allowance of claims 3-6 and 8-10.

Drawings

Applicants submit herewith corrected formal drawings, under cover of a separate Transmittal of Formal Drawings. Applicants respectfully request approval of the corrected formal drawings, which now reference FIG. 2 as "PRIOR ART" as requested by the Examiner and as previously proposed in a red-marked copy of the drawing figured filed with a separate transmittal letter to the Chief Draftsman in conjunction with the Amendment filed January 9, 2002.

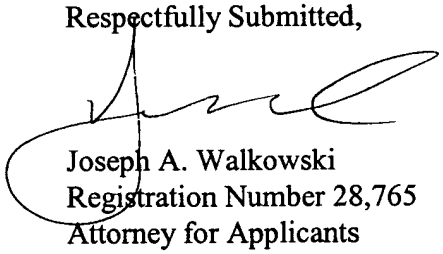
ENTRY OF AMENDMENT

The amendment to claim 2 should be entered as it is supported by the as-filed specification and drawings of the present application. Further, it is to be noted that no surrender of scope of claim 2 or any other claim herein is to be understood by the amendment as set forth, the purpose for same being solely to assist the Examiner in recognizing that the claimed semiconductor device is separate and distinct from any carrier substrate to which it may be operably coupled.

CONCLUSION

It is respectfully submitted that claims 1 through 10 are in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,



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JAW/ps:dlm
Date: July 29, 2002
Enclosure: Version With Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

2. (Amended) A semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising:

a semiconductor substrate;

active circuit devices on the semiconductor substrate; and

a capacitor having at least a portion thereof formed in an active area of the semiconductor substrate, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance for the semiconductor device when the semiconductor device is operably connected to the [a] carrier substrate.